Claims

[c1] What is claimed is:

1.A charge pump and loop filter circuit of a phase locked loop, comprising:

a first input current source electrically connected to a first node of the circuit supplying a first current to the circuit, the first current being equal to a predetermined amount of current multiplied by a first factor;

a second input current source electrically connected to a second node of the circuit for supplying a second current to the circuit, the second current being equal to the predetermined amount of current multiplied by a second factor;

a first output current source electrically connected to a third node of the circuit for outputting the first current from the circuit;

a second output current source electrically connected to a fourth node of the circuit for outputting the second current from the circuit;

a unit gain buffer electrically connected between an intermediate node and a fifth node of the circuit for supplying a voltage of the intermediate node to the fifth node;

a first capacitor electrically connected between the intermediate node of the circuit and ground;

a resistor electrically connected between the fifth node and an output node of the circuit;

a plurality of up pulse switches controlled by an up pulse control signal for controlling current flow such that in a charging mode of the circuit, the second current flows from the second node through the output node and through the resistor to the fifth node, and the first current flows from the first node through the intermediate node to the first capacitor for charging the first capacitor; and

a plurality of down pulse switches controlled by a down pulse control signal for controlling current flow such that in a discharging mode of the circuit, the second current flows from the fifth node through the resistor and out through the second output current source, and the first current flows from the first capacitor through the intermediate node and out through the first output current source for discharging the first capacitor.

[c2] 2.The circuit of claim 1 wherein the circuit further comprises a second capacitor

electrically connected between the output node of the circuit and ground.

[c3] 3.The circuit of claim 1 wherein the plurality of up pulse switches comprises a first up pulse switch and a second up pulse switch, the first up pulse switch being connected between the first node and the intermediate node, and the second up pulse switch being connected between the second node and the output node, and the plurality of down pulse switches comprises a first down pulse switch and a second down pulse switch, the first down pulse switch being connected between the intermediate node and the third node, and the second down pulse switch being connected between the output node and the fourth node.

[c4] 4.The circuit of claim 3 wherein when the up pulse control signal is active and the circuit is in the charging mode, the first and second up pulse switches close and the first and second down pulse switches open, and when the down pulse control signal is active and the circuit is in the discharging mode, the first and second down pulse switches close and the first and second up pulse switches open.

[c5] 5.The circuit of claim 1 wherein the first factor is less than one and the second factor is equal to one.

[c6] 6.The circuit of claim 1 wherein the up pulse switches and the down pulse switches are transistors.

[c7] 7.The circuit of claim 1 wherein the unit gain buffer is a source follower or an emitter follower.

[c8] 8.The circuit of claim 1 wherein the unit gain buffer is an operational amplifier with direct feedback, forming a voltage follower.

[c9] 9.A charge pump and loop filter circuit of a phase locked loop, comprising:
a first input current source electrically connected to a first node of the circuit supplying a first current to the circuit, the first current being equal to a predetermined amount of current multiplied by a first factor;
a second input current source electrically connected to a second node of the

circuit for supplying a second current to the circuit, the second current being equal to the predetermined amount of current multiplied by a second factor;
a first output current source electrically connected to a third node of the circuit for outputting the first current from the circuit;
a second output current source electrically connected to a fourth node of the circuit for outputting the second current from the circuit;
a first capacitor electrically connected between an output node and an intermediate node of the circuit;
a resistor electrically connected between the intermediate node and a reference node of the circuit;
a plurality of up pulse switches controlled by an up pulse control signal for controlling current flow such that in a charging mode of the circuit, the second current flows from the second node to the intermediate node, the first current flows from the first node through the output node and through the first capacitor to the intermediate node for charging the first capacitor, and a sum of the first current and the second current flows from the intermediate node through the resistor and out through the reference node; and
a plurality of down pulse switches controlled by a down pulse control signal for controlling current flow such that in a discharging mode of the circuit, the sum of the first current and the second current flows from the reference node through the resistor to the intermediate node, the second current flows from the intermediate node and out through the second output current source, and the first current flows from the intermediate node through the first capacitor and out through the first output current source for discharging the first capacitor.

[c10] 10.The circuit of claim 9 wherein the circuit further comprises a second capacitor electrically connected between the intermediate node and the reference node of the circuit.

[c11] 11.The circuit of claim 9 wherein the plurality of up pulse switches comprises a first up pulse switch and a second up pulse switch, the first up pulse switch being connected between the first node and the output node, and the second pulse switch being connected between the second node and the intermediate

node, and the plurality of down pulse switches comprises a first down pulse switch and a second down pulse switch, the first down pulse switch being connected between the output node and the third node, and the second down pulse switch being connected between the intermediate node and the fourth node.

[c12] 12.The circuit of claim 11 wherein when the up pulse control signal is active and the circuit is in the charging mode, the first and second up pulse switches close and the first and second down pulse switches open, and when the down pulse control signal is active and the circuit is in the discharging mode, the first and second down pulse switches close and the first and second up pulse switches open.

[c13] 13.The circuit of claim 9 wherein the first and second factors are values less than one, and a sum of the first and second factors equals to one.

[c14] 14.The circuit of claim 9 wherein the up pulse switches and the down pulse switches are transistors.

[c15] 15.A charge pump and loop filter circuit of a phase locked loop, comprising:
a first input current source electrically connected to a first node of the circuit supplying a first current to the circuit, the first current being equal to a predetermined amount of current multiplied by a first factor;
a second input current source electrically connected to a second node of the circuit for supplying a second current to the circuit, the second current being equal to the predetermined amount of current multiplied by a second factor;
a first output current source electrically connected to a third node of the circuit for outputting the first current from the circuit;
a second output current source electrically connected to a fourth node of the circuit for outputting the second current from the circuit;
an operational amplifier, a first input of the operational amplifier being electrically connected to a fifth node of the circuit, a second input of the operational amplifier being electrically connected to a reference node of the circuit, and an output of the operational amplifier being electrically connected to an output node of the circuit;

a first capacitor electrically connected between the fifth node and an intermediate node of the circuit;

a resistor electrically connected between the intermediate node and the output node of the circuit;

a plurality of up pulse switches controlled by an up pulse control signal for controlling current flow such that in a charging mode of the circuit, the second current flows from the second node to the intermediate node, the first current flows from the first node through the fifth node and through the first capacitor to the intermediate node for charging the first capacitor, and a sum of the first current and the second current flows from the intermediate node through the resistor and out through the output node; and

a plurality of down pulse switches controlled by a down pulse control signal for controlling current flow such that in a discharging mode of the circuit, the sum of the first current and the second current flows from the output node through the resistor to the intermediate node, the second current flows from the intermediate node and out through the second output current source, and the first current flows from the intermediate node through the first capacitor to the fifth node and out through the first output current source for discharging the first capacitor.

[c16] 16.The circuit of claim 15 wherein the circuit further comprises a second capacitor electrically connected between the intermediate node and the output node of the circuit.

[c17] 17.The circuit of claim 15 wherein the plurality of up pulse switches comprises first up pulse switch and a second up pulse switch, the first up pulse switch being connected between the first node and the fifth node, and the second up pulse switch being connected between the second node and the intermediate node, and the plurality of down pulse switches comprises a first down pulse switch and a second down pulse switch, the first down pulse switch being connected between the fifth node and the third node, and the second down pulse switch being connected between the intermediate node and the fourth node.

[c18] 18.The circuit of claim 17 wherein when the up pulse control signal is active and the circuit is in the charging mode, the first and second up pulse switches close and the first and second down pulse switches open, and when the down pulse control signal is active and the circuit is in the discharging mode, the first and second down pulse switches close and the first and second up pulse switches open.

[c19] 19.The circuit of claim 15 wherein the first and second factors are values less than one, and a sum of the first and second factors equals to one.

[c20] 20.The circuit of claim 15 wherein the up pulse switches and the down pulse switches are transistors.